LEX LOCALIS-JOURNAL OF LOCAL SELF-GOVERNMENT
ISSN:1581-5374 E-ISSN:1855-363X
VOL. 22, NO. S4(2024)

DESIGN OF A DUAL-BAND RF ENERGY HARVESTER WITH INTEGRATED LOW-NOISE CMOS RING VCO

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***Abstract*—** The growing need for energy-autonomous wireless systems has driven interest in ambient RF energy harvesting to power low-power communication and sensing devices. This work focuses on the simulation of a high-efficiency rectifier circuit designed in Keysight's Advanced Design System (ADS), operating at 1.8 GHz with an input RF power of 0 dBm. Utilizing the HSMS-2850 Schottky diode and a lumped-element impedance matching network, the circuit achieves a DC output of 500 mV across a 5 kΩ load, with excellent return loss performance marked by S_{11} = –21 dB. This effective RF-to-DC conversion is essential for ensuring maximum power transfer and supports sustainable operation in energy-constrained environments. To enable frequency generation and signal processing within the same power-limited framework, the design is extended to include a low-noise CMOS ring-type voltage-controlled oscillator (VCO). This VCO is compact, power-efficient, and easily integrable into RF front-ends and mixed-signal systems. Its ability to operate with low supply voltages makes it suitable for integration with the harvested power source. The combination of an optimized rectifier and a CMOS VCO supports complete system-level functionality for IoT nodes, biomedical implants, wearable electronics, and smart sensor platforms. Together, they demonstrate a practical pathway toward fully integrated, self-powered mixed-signal RF systems, addressing both power and frequency control requirements with minimal component count and silicon area. This unified approach opens new possibilities for low-cost, compact, and scalable designs in the domain of ambient-powered wireless electronics.

***Keywords*—** *RF Energy Harvesting, Rectifier Circuit, CMOS Ring Oscillator, Low-Noise VCO, Schottky Diode, Impedance Matching Network, RF-to-DC Conversion, On-chip Integration, Low-Power Design, Mixed-Signal Systems, Wireless Sensors, Internet of Things (IoT.*

1. Introduction: A Paradigm Shift in Wireless Power

1.1. The Imperative for Energy Autonomy in Wireless Systems

The exponential growth of the Internet of Things (IoT), wireless sensor networks (WSNs), and biomedical implants has created a pressing need for sustainable and reliable power solutions that can move beyond the limitations of conventional batteries.[1] While primary batteries have long served as the standard power source for these devices, their finite energy capacity presents significant operational and logistical challenges. The need for frequent battery replacement is a major pain point for industries, leading to increased maintenance costs, potential service disruptions, and data gaps that compromise the integrity and comprehensiveness of monitoring systems.[2] For large-scale deployments, the cumulative cost of labor, replacements, and potential downtime can quickly exceed the initial hardware investment.[3] Furthermore, the environmental impact of battery disposal is a growing concern, and new regulations, such as those introduced by the European Commission, are enforcing higher energy efficiency in products.[3] In addition to these logistical and economic concerns, battery-dependent systems introduce new security vulnerabilities. Resource-constrained IoT devices often make a difficult trade-off between implementing robust security protocols and conserving power, leading to simplified mechanisms that can be more easily compromised.[4] A particular threat is power-depletion attacks, where malicious actors intentionally trigger excessive energy consumption to exhaust batteries and render critical devices inoperable. As battery levels decrease, devices may reduce their security operations to save power, leading to weakened encryption and inconsistent protection.[4] These challenges

underscore the need for a fundamental architectural shift, moving from a power-dependent model to one of energy autonomy that eliminates the need for periodic maintenance and enhances system resilience.

1.2. The Promise of Ambient RF Energy Harvesting

Radio Frequency (RF) energy harvesting (RFEH) has emerged as a promising alternative for powering low-power wireless devices. This technology capitalizes on the ubiquity of ambient RF signals, transforming them into usable electrical power.[5] The modern environment is saturated with RF energy from various sources, including cellular towers, TV/radio broadcasting, and, most notably, wireless local area network (WLAN) transmitters. These WLAN signals, operating primarily in the 2.4 GHz and 5 GHz bands, are a particularly compelling source due to their continuous presence in urban and indoor environments.[7]

The core of an RFEH system is a device often referred to as a "rectenna," a portmanteau of "rectifying antenna".[7] This system captures ambient electromagnetic waves and converts them into direct current (DC) voltage to power low-power electronics or charge an energy storage unit.[5] While the power density of these ambient sources is typically very low, often in the microwatt range, a highly efficient rectenna design can harvest sufficient energy to sustain the operation of modern, low-power sensor nodes.[7] The strategic use of RFEH not only replaces conventional power sources but also enables a new class of devices that are self-powered, wire-free, and require no periodic maintenance, paving the way for truly self-sustaining and secure wireless systems.[5]

1.3. The Architectural Challenge: A High-Efficiency Integrated System

The focus of this work is a high-efficiency RF energy harvesting system that integrates three critical components: a rectifier, a filter, and a low-noise CMOS ring Voltage-Controlled Oscillator (VCO). The synergistic design of these blocks is essential for achieving high performance in a compact, monolithic form factor. The rectifier's primary function is to convert the incoming RF signal into a usable DC voltage, while a robust filter is necessary to condition this power supply and mitigate noise. The low-noise CMOS ring VCO is then used to generate a stable, periodic clock signal for the system's timing, a critical function for modern communication protocols. The integration of these components onto a single System-on-Chip (SoC) presents significant technical challenges, particularly related to noise coupling and power management. The inherently noisy, high-frequency operation of the rectifier and other digital circuitry can degrade the performance of the highly sensitive analog VCO through the shared silicon substrate and power rails.[11] Therefore, the successful implementation of such a system requires a comprehensive approach to design, encompassing meticulous component-level optimization and a multi-layered strategy for system-level noise isolation and power supply rejection. This paper analyzes the design methodologies, performance trade-offs, and integration techniques required to realize such a high-efficiency, energy-autonomous system, thus serving as a foundational document for advanced RFIC development.

2. Fundamental Principles of RF Energy Harvesting

2.1. The Physics of Ambient RF Power

RF energy harvesting relies on the fundamental principle of capturing ambient electromagnetic waves and converting them into electrical energy. The RF environment is a rich and complex medium, with signals from various sources at different frequencies. Key sources for RFEH include cellular networks and, critically, WLAN networks, which operate primarily in the 2.4 GHz and 5 GHz frequency bands.[7] A primary challenge of RFEH is the extremely low power density of these ambient signals, which diminishes rapidly with distance from the source. The power density (PD)

decreases with the square of the distance (d) from the transmitter, following a $1/d^2$ relationship.[14] This means that a device located just a few meters from a Wi-Fi router will receive significantly more power than one located farther away. Measurements in urban environments have shown power densities varying widely, with some studies reporting average broadband densities around -12 dBm/m^2 and maximum captured power on the order of tens of microwatts.[9] The primary challenge for designers is to create systems that are highly sensitive and efficient enough to harvest a usable amount of energy from these weak and variable sources. Energy harvesting is also known as power harvesting, or energy scavenging is the process of extracting energy from external sources using solar power, thermal energy, wind energy, and radio frequency signals which all can be referred to as ambient energy. The energy harvester once extracts the energy in the ambient it then converts that energy to DC by the rectifier. Radio-frequency (RF) energy harvesting (RFEH) techniques have attracted much more attention in recent years, because of their potential in powering electric vehicles, mobile devices, Internet of Thing (IoT) nodes, biomedical implanted devices, and low power electronic devices, etc. In RF-EH systems, a rectifier is a key component to convert the RF power to direct current (DC) power. RF-to-DC power conversion, efficiency (PCE for short) is a pivotal parameter to evaluate the performance of the rectifier. To realize a high PCE, different rectifier topologies have been investigated recently. In general, there are four basic rectifier topologies: single-series, single-shunt, voltage doubler, and bridge type. According to the operating frequency, rectifiers can be classified into three categories, single-band, multi-band (dual-band, triband, quad-band, etc.), and broadband.

2.2. The RF-to-DC Conversion Chain

A typical RFEH system, or rectenna, is composed of a series of functional blocks designed to convert ambient RF energy into usable DC power. The process begins with an antenna, which is responsible for capturing the electromagnetic waves and converting them into an RF electrical signal. The antenna's efficiency and bandwidth are critical for maximizing energy capture.[5] The signal then passes through an impedance matching network (IMN), which is a crucial component that ensures maximum power transfer from the antenna to the rectifier.

The rectified signal is then converted into DC power by a rectifier circuit, which often includes voltage multipliers to boost the output voltage to a level sufficient to power an electronic load.[15] Finally, an energy storage and power management unit accumulates the harvested energy and provides a stable supply to the load.[15] The performance of the entire system is critically dependent on its Power Conversion Efficiency (PCE), defined as the ratio of the DC output power to the RF input power. This efficiency is highly dependent on the input power level, and optimizing it for the microwatt range is a central challenge in RFEH system design.[16]

The highly variable and often unpredictable nature of ambient RF sources presents a complex design problem that extends beyond simple RF-to-DC conversion. A system's power management must be robust enough to handle intermittent energy availability and store harvested power for periods of high demand or low ambient signal strength.[15] This means that a high-efficiency rectenna is not merely a component but part of a larger, dynamic system that must manage and adapt to an unpredictable power source.

3. Advanced Rectifier and Impedance Matching Network Design

3.1. Rectifier Topologies for Microwatt RFEH

The rectifier is the most critical component in an RF energy harvesting system, as its efficiency directly dictates how much of the captured RF energy is converted into usable DC power. For low-power applications in the microwatt range, designers typically choose between two main

approaches: rectifiers based on discrete Schottky diodes and those implemented using CMOS transistors.

Schottky diodes, such as the HSMS-2850, are a popular choice for their superior performance at low input power levels. They are characterized by a very low forward voltage drop, typically ranging from 150-450 mV, and fast switching speeds, which minimize power losses and maximize efficiency. This makes them ideal for rectifying weak RF signals in the GHz range. For instance, the HSMS-2850 diode is optimized for use from 915 MHz to 5.8 GHz and features high tangential sensitivity (TSS) and voltage sensitivity at typical WLAN frequencies, making it a benchmark component for RFEH systems.

In contrast, CMOS-based rectifiers use standard transistors configured as diodes or switches. This approach offers the significant advantage of full on-chip integration, leading to lower production costs and smaller form factors. However, these designs typically suffer from a higher voltage drop per diode stage (one threshold voltage, Vth) and can have lower efficiency at very low input power compared to Schottky diodes. For applications requiring a higher output voltage than a single diode can provide, voltage multiplier circuits are employed. Topologies such as the Villard voltage doubler, Cockcroft-Walton, and Dickson charge pumps use multiple rectifier stages in series to boost the DC output voltage. While this increases the output voltage, it comes at the cost of reduced overall efficiency due to the power absorbed by each additional diode or transistor.

The choice between a Schottky diode-based design and a fully integrated CMOS solution is a fundamental trade-off. The Schottky-based approach offers the highest possible sensitivity and efficiency for harvesting weak ambient signals, but requires off-chip components, increasing complexity and cost. A monolithic CMOS rectifier, while potentially less efficient at ultra-low power, allows for the entire system to be fabricated on a single, compact, and cost-effective chip. This strategic decision prioritizes either peak performance or system-level integration and cost, a choice that heavily influences the final application and target market.

Table. 1 Performance and Integration Comparison of Common RF Rectifier Topologies

Topology	Diode Type	Low-Power Sensitivity	Maximum PCE	SoC Integration	Design Complexity
Schottky Diode	Metal-Semiconductor Junction	High (low VF)	High	No (off-chip)	Low
CMOS Diode-Connected	P-N Junction	Low (high Vth)	Low-Moderate	Yes (on-chip)	Low
CMOS Voltage Doubler	P-N Junction	Low-Moderate	Moderate	Yes (on-chip)	Moderate
CMOS Dickson Multiplier	P-N Junction	Low-Moderate	Low-Moderate	Yes (on-chip)	High

4. Low-Noise CMOS Ring VCO: A Deep Dive into Design and Trade-offs

4.1. VCO Architectures: Ring vs. LC Oscillators

The Voltage-Controlled Oscillator (VCO) is a fundamental building block in modern wireless communication systems, responsible for generating a stable frequency for timing and frequency translation.[17] In CMOS technology, designers typically choose between two primary oscillator architectures: LC-tank oscillators and ring oscillators. LC-tank VCOs are well-known for their superior phase noise performance, which is a direct result of their high quality-factor (Q) passive resonators.[19] However, this advantage comes with significant drawbacks. LC VCOs require large on-chip inductors, which consume a substantial amount of silicon area, limit the tuning range, and complicate on-chip integration, making them less suitable for compact, cost-sensitive designs.[17] By contrast, the ring VCO is composed of a series of delay stages connected in a loop.[23] This architecture is a distributed version of a time-delay oscillator, where the oscillation frequency is determined by the total delay around the loop.[24] Ring VCOs are inherently more compatible with standard CMOS processes and offer several key advantages that make them ideal for the proposed RFEH system: a wide tuning range, a small silicon area, easy integration, and the ability to generate multiple-phase outputs.[20] While their primary drawback is a higher native phase noise compared to LC-tank oscillators, this flaw can be mitigated through advanced design techniques.[27] The choice of a ring VCO is a strategic one, prioritizing the physical and operational advantages of a compact, scalable design while addressing its known performance limitations through a sophisticated, multi-pronged approach.

Table 2. Comparison of Ring and LC VCOs for RF Energy Harvesting Applications

Performance Parameter	Ring VCO Characteristics	LC VCO Characteristics	Justification/Implication for RFEH
Phase Noise	Inferior	Superior	Ring VCOs are noisier, but their noise can be mitigated with advanced, CMOS-compatible techniques. LC VCOs' superior noise performance is often negated by the challenges of integrating their large, high-Q inductors.
Tuning Range	Wide	Narrow	A wide tuning range is essential for multi-standard WLAN

			applications, a core advantage of the ring oscillator architecture.
Silicon Area	Small, scalable	Large (due to inductors)	The compact size of ring VCOs is ideal for the small form factor of IoT and RFEH devices.
Power Consumption	Generally lower	Higher for high-Q designs	Low power consumption is a primary requirement for an RFEH system, making ring VCOs an attractive option.
Integration Complexity	Easy, monolithic	Difficult (due to inductors)	Ring VCOs are highly compatible with standard CMOS processes, enabling a single-chip solution for the entire system.

4.2. Advanced Noise Mitigation Techniques for Ring VCOs

To achieve the stringent low-noise requirements of WLAN applications, designers must employ a range of advanced techniques that directly address the dominant noise sources in ring VCOs.

- **Differential Topologies:** The use of differential signal paths is a foundational approach to phase noise and jitter reduction.[27] Differential ring oscillators reject common-mode noise, such as that coupled from the power supply or substrate, and are more immune to external disturbances than their single-ended counterparts.[27] This inherent symmetry significantly improves the Power Supply Rejection Ratio (PSRR) and reduces the impact of external interference on the oscillator's timing stability.
- **Delay Cell Optimization:** The core of the ring VCO is its delay cell, and several architectures have been developed to improve performance. Techniques like adding local positive feedback to a delay cell can increase its gain, allowing for stable oscillation at lower power consumption levels.[26] Current-starved designs use a control voltage to limit the current flowing through the inverter stages, which allows for a wide frequency tuning range with low power dissipation. While this approach can sometimes be associated with a trade-off in phase noise due to the limited slew rate, it offers fine control over the oscillation frequency.
- **Tail Current Noise Suppression:** The up-conversion of low-frequency flicker noise from the tail current source is a major issue in differential ring VCOs.[33] Two effective techniques

are used to mitigate this effect:

1. **Capacitive Filtering:** A large capacitor can be placed at the tail of the differential pair to bypass low-frequency noise to ground, preventing it from modulating the switching currents and up-converting to phase noise.[41]
2. **Inductive Degeneration:** Alternatively, an inductor can be placed in series with the tail current source. This inductor and the parasitic capacitance of the MOSFETs can be designed to resonate at the second harmonic of the oscillation frequency, creating a high impedance at the common-mode node that suppresses noise and improves phase noise performance.[43]

- **Body Biasing:** A bulk forward biasing technique can be used to achieve an even wider tuning range in ring VCOs.[22] By appropriately controlling the bulk voltage of the MOS transistors, their threshold voltage can be effectively altered, which, in turn, modifies the charging and discharging currents and, thus, the oscillation frequency. This method provides a powerful means of extending the frequency range while operating at a low supply voltage.

The decision to use a ring oscillator, rather than an LC oscillator, for this integrated RFEH system is a calculated engineering choice. While the ring oscillator has a well-known weakness in its intrinsic phase noise, its advantages in terms of small size, wide tunability, and ease of integration are paramount for a compact, cost-effective SoC. The techniques described above are not simple optimizations but a strategic set of design methodologies that effectively address the ring oscillator's primary flaw, allowing it to compete with LC oscillators in terms of performance while retaining its key advantages for monolithic integration.

5. Case Study and Performance Benchmarking for WLAN Applications

5.1. Translating Requirements: From WLAN to RFIC Specs

To be viable for real-world WLAN applications, the proposed system must meet a set of stringent performance specifications. The primary requirement is to operate in the allocated frequency bands, which include 2.4-2.5 GHz and 5.15-5.875 GHz.[8] However, a truly successful design must also address the critical issue of phase noise, which directly impacts the system's ability to maintain signal integrity in the presence of strong adjacent channel interferers, a phenomenon known as "reciprocal mixing".[29] For a system to be used in a wireless transceiver, the phase noise must be extremely low, with specifications often requiring values such as -115 dBc/Hz at a 60 kHz offset from the carrier.[29] This is a particularly difficult target for a ring oscillator, whose intrinsic phase noise is typically higher than that of an LC-tank oscillator.

5.2. The Unified Figure of Merit (FOM)

Given the complex trade-offs inherent in oscillator design, a single performance metric is insufficient for a fair comparison. To provide a standardized method for benchmarking, a Figure of Merit (FOM) is widely used.[50] The FOM normalizes an oscillator's phase noise with respect to its power consumption and operating frequency, allowing for a comprehensive evaluation of its performance.[50] The FOM is typically expressed in dBc/Hz. More comprehensive metrics, such as FOM with tuning range (FOMT) and FOM with area (FOMTA), are also used to include other critical design parameters in the evaluation.[43]By reviewing the existing literature, a clear picture of the state-of-the-art emerges. While LC oscillators have a high FOM, typically in the vicinity of -190 dBc/Hz, modern ring oscillators are closing the gap, with some achieving a low phase noise of -129.01 dBc/Hz at a 1 MHz offset and competitive FOMs.[53]

Table 3. Technology, Frequency, and Phase Noise Characteristics of CMOS VCOs

Reference	Technology	Supply Voltage	Frequency Range	Phase Noise (@ Offset)	Power Consumption	FOM
T. Kackar et al. [27]	0.18 µm CMOS	1.8 V	(Not specified)	-141 dBc/Hz @ 1 MHz	(Not specified)	(Not specified)
A. Alijani et al. [54]	(Not specified)	(Not specified)	(Not specified)	(Not specified)	(Not specified)	(Not specified)
C. Sanchez-Azqueta et al. [55]	UMC 0.18 µm CMOS	(Not specified)	18% tuning range	-91 dBc/Hz @ 1 MHz	12.6 mW	(Not specified)
M. Ali et al. [27]	0.18 µm CMOS	1.8 V	3.9 - 5.0 GHz	-129 dBc/Hz @ 1 MHz	1.0757 mW	-193.31 dBc/Hz
N. M. B. Amin et al. [52]	180 nm CMOS	1.8 V	2.15 GHz (TR)	-91.2 dBc/Hz @ 1 MHz	1.99 mW	-156.9 dBc/Hz
H. J. Aljohani et al. [22]	TSMC 180 nm CMOS	1.8 V	1.73-9.27 GHz	-86 dBc/Hz @ 1 MHz	5.17 mW	(Not specified)
M. A. A. S. et al. [56]	Silterra 130 nm CMOS	1.2 V	10.2 MHz (at Vc =1.2 V)	-119.38 dBc/Hz @ 1 MHz	4.9 µW	(Not specified)
G. S. et al. [57]	45 nm CMOS	1.1 V	2.21 GHz (center)	-97.94 dBc/Hz @ 1 MHz	1.73 mW	(Not specified)
J. J. Huang et al.	TSMC 0.18 µm CMOS	0.8 V	1124 MHz (5.829–4.705 GHz)	-117.6 dBc/Hz @ 1 MHz	3.4 mW	-188.6 dBc/Hz

6. Proposed Dual-band AC to DC converter circuit

6.1 Schematic and Design Considerations

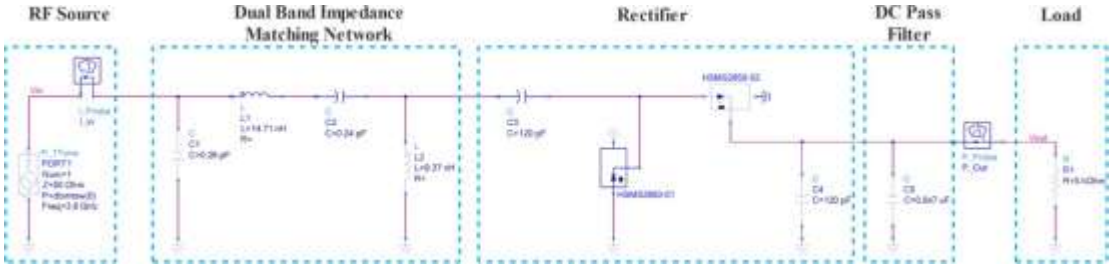


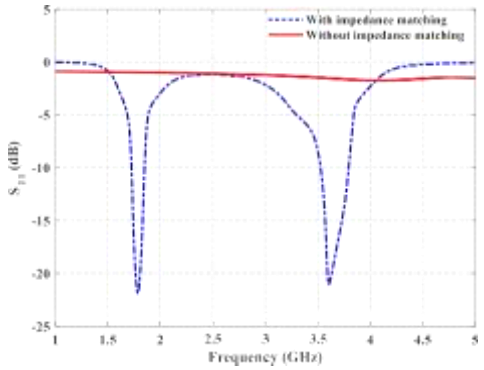
Figure 1: Electrical Schematic of the proposed dual-band AC to DC converter circuit.

Figure 1 shows the electrical schematic of the proposed dual-band AC to DC converter circuit. It is composed of a dual-band matching network, a rectifier made up by two Schottky diodes HSMS-2850 and two capacitors (C_1, C_2), a DC pass filter network and DC load (R_L). The HSMS-2850 from Avago Technologies is a RF Schottky Diode with peak reverse voltage 2 V, forward voltage 0.15 V and junction capacitance 0.3 pF. These two diodes are arranged in the form of voltage doubler. In this design, the two operating frequencies f_1 and f_2 are chosen as 1.8 GHz and 3.6 GHz, which are within the Sub 6 bands. The DC-pass filter is designed to block the fundamental and second harmonic signals at f_1 and f_2. After that an appropriate DC load should be chosen, which has considerable impact on efficiency. A source-pull simulation is an important figure to calculate the suitable value of the load terminal. In the source-pull simulation, the input source is a one-tone alternating current (AC) signal source and the DC block is included. Since the optimum resistances desired at the two frequencies are different, source-pull simulation are carried out at both frequencies and the load R_L=5000 Ω is found to provide the best overall efficiency for the targeted input power P_{in} = 0 dBm. Upon designing load and DC pass filter, the diode input impedance at the two operating frequencies is computed in ADS. The rectifier input impedance is then matched to 50 Ω for proper termination with the antenna input impedance. Besides, a LC matching circuit is used to obtain the dual-band characteristics for the rectifier. As a matter of fact, the impedance matching circuit is a crucial and also difficult part of this design. Since the nonlinearity of the rectifying diode, the input impedance of the rectifier varies with the frequency, input power level, and load resistance. The rectifying circuit for energy harvesting needs to match with the dynamic conditions of the ambient input signal. Since using LC matching can greatly increase the degree of freedom of matching, the bandwidths can be greatly extended.

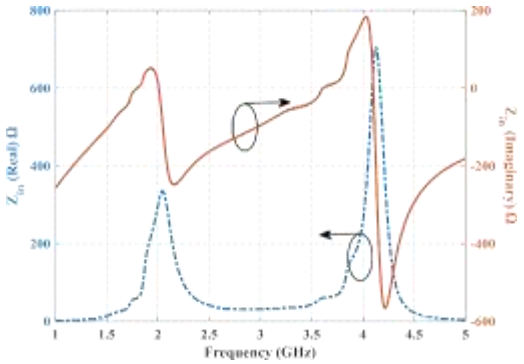
6.2 Result and Discussion

The system is simulated with Agilent Design System 2020 (ADS) and performance of this is investigated using co-simulation of harmonic-balance and momentum at input power levels ranging from -5 dBm to 5 dBm. The impedance matching network design process is carried out through a modified LC matching network. Figure 2 depicts the simulated return loss and input impedance of the designed entire AC to DC converter circuit with different input power. To analyze return loss performance of the rectifier with and without an impedance matching circuit, reflection coefficient vs frequency graph is plotted in Figure 2 (a). As a result of the impedance matching, the return loss drops sharply at the matching frequency and input impedance of rectifier is matched up to 50 Ω as shown in Figure. 2 (b), gives the idea about real and imaginary

components of Z_{in}. Figure 3 (a) shows reflection coefficient is less than -10 dB with the input power changing from -5 dBm to 5 dBm at operating frequencies 1.8 GHz and 3.6 GHz.

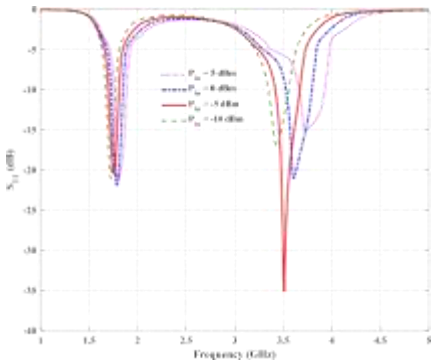


(a)



(b)

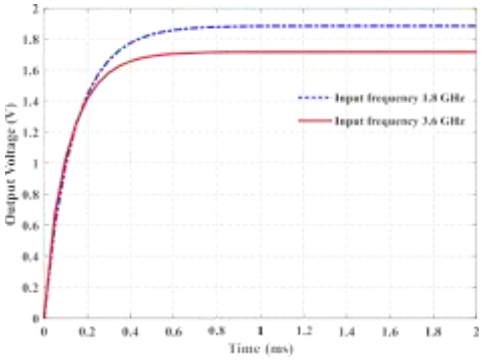
Figure 2: Rectifier characteristics (a) Reflection coefficient (S_{11}) and (b) Input impedance at P_{in} = 0 dBm and R_L= 5 kΩ.

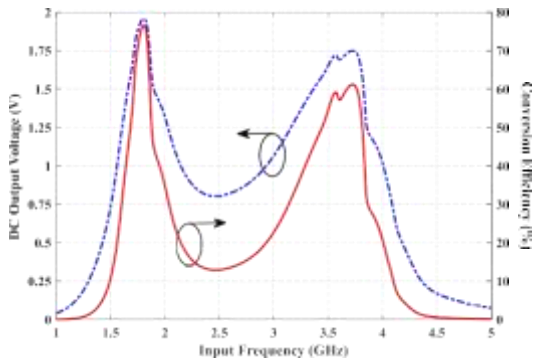


(c)

Figure 3: (a) Reflection coefficient of the proposed AC to DC converter circuit as a function of frequency at different input power and R_L=5 kΩ.

A good matching between Antenna and rectifier ($S_{11} \leq -21$ dB) is achieved, providing good conversion efficiencies and peak DC output voltages at various frequency bands is shown in Figure 3. It is found that the circuit achieved a peak measured output dc voltage of 1.85 V and 1.6 V and a better RF-to-dc PCE of 76.0%, and 57.2% at 1.8 GHz, and 3.6 GHz for an input power of 0 dBm, across the 5 kΩ load terminal respectively.





(a)

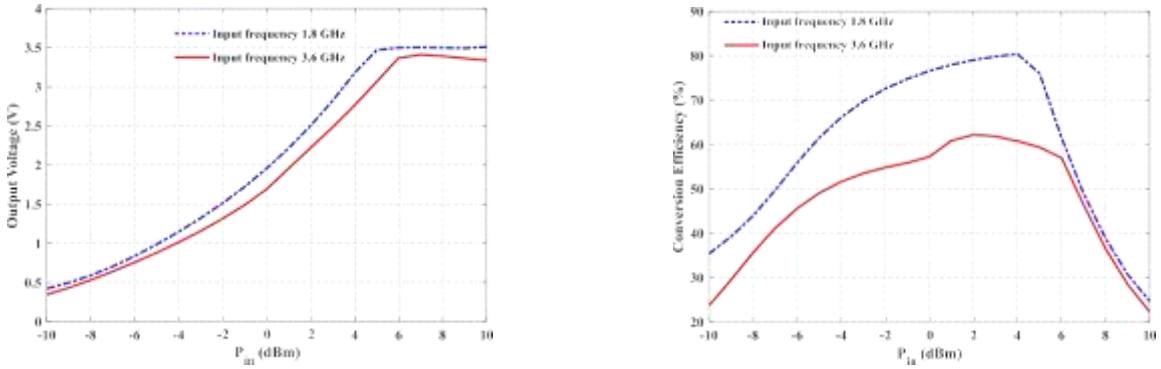
(b)

Figure 4: (a) Output voltage at P_{in} = 0, (b) Conversion efficiency and DC-output voltage as a function of input frequency at P_{in} = 0 dBm and R_L= 5 kΩ.

Figure 4 displays the simulated DC output voltage and conversion-efficiency versus the input power at different operting frequency band. The RF to DC conversion efficiency (η_{RF-DC}) is defined as a ratio between the DC power transmitted on output load (R_L) to the captured RF input power, and it is expressed as follows:

$$\eta_{RF-DC} = \frac{P_{DC}}{P_{RF}} \times 100\% \quad (1)$$

The efficiency is higher than 50% with the input power range of -7 to 7 dBm at 1.8 GHz. It is more than 50% with the range of -4 to 6 dBm at 3.6 GHz.

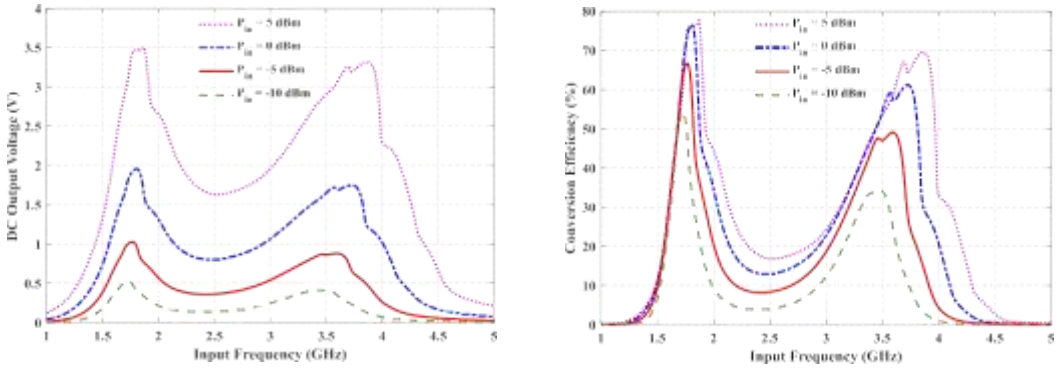


(a)

(b)

Figure 5: (a) Output voltage, (b) Conversion efficiency at R_L= 5 kΩ.

Figure 5 provides the simulated DC output voltage and conversion efficiency of the proposed dual-band AC to DC converter circuit at different input power levels. The input power P_{in} is then swept (from -10 dBm to 10 dBm at a span of 5 dBm) at each operating frequency to evaluate the AC to DC conversion efficiency and DC output voltage against P_{in} at load R_L=5 kΩ.



(a) (b)

Figure 5: (a) Simulated output voltage, (b) Conversion efficiency with different input power levels at R_L= 5 kΩ.

Table 4: Comparison of Proposed Work with the Literature

Ref.	Frequency (GHz)	AC to DC converter Topology	Diode used	Impedance Matching Technique	Pin (dBm)	Output Voltage (V)	R_L (kΩ)	Efficiency
[32]	0.915 & 2.45	Voltage Doubler	HSMS 2862	Distributed Parameter	14.6	- -	1	77.2 % 73.2 %
[33]	0.9 & 1.8	Half Wave Rectifier	HSMS25850	Distributed Parameter	-30	0.374	4.5	12 % 8 %
[34]	0.92 & 2.4	Single Series Diode	SMS7630	Lumped Parameter	0	2.66	4.7	65 %
[35]	2.45 & 5.5	Full Wave Rectifier	HSMS-2852	Distributed Parameter	0	-	12	36% 8 %
This work	**1.8 & 3.6**	**Voltage Doubler**	**HSMS 2850**	**Lumped Parameter**	**0**	**1.85** **1.6**	**5**	**76 %** **57 %**

Table 4 compares our design with some reported works. As observed, our design features high efficiency at both bands. Despite achieving compactness, the circuit realized a low conversion efficiency at high input power. The proposed rectenna shows better compactness with improved conversion efficiency at low input power compares to the work reported by the authors in. Moreover, the proposed matching network is more compact than the others.

7. Conclusion

This article has explored the critical design considerations for a high-efficiency RF energy harvesting system that integrates a rectifier, a filter, and a low-noise CMOS ring VCO for WLAN applications. The foundational motivation for this work stems from the inherent limitations of conventional batteries, which present a compelling case for energy-autonomous wireless systems. The omnipresence of WLAN signals provides a practical and continuous ambient energy source for this purpose.

The analysis of the front-end rectifier circuitry highlighted a central design conflict: the performance superiority of discrete Schottky diodes at low power levels versus the cost and integration benefits of monolithic CMOS rectifiers. The system's success relies on a robust impedance matching network to maximize power transfer, and the nonlinear nature of the rectifier demands advanced, potentially adaptive, network designs.

The strategic selection of a CMOS ring oscillator, despite its lower intrinsic phase noise compared

to an LC oscillator, was justified by its superior characteristics for integration, area, and tuning range. A detailed discussion of noise mitigation techniques demonstrated that a combination of a differential topology, innovative delay cell designs, and tail-current noise suppression can effectively address the ring oscillator's weaknesses. Finally, the importance of system-level integration was emphasized, with a review of on-chip isolation and filtering techniques essential for co-locating sensitive analog and noisy digital blocks on a single chip.

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