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MAXIMIZING PHOTOVOLTAIC EFFICIENCY USING INTERLEAVED DC-DC CONVERTERS AND ASYMMETRICAL NINE-LEVEL INVERTER CONFIGURATION

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ABSTRACT: This paper presents a new method based on the integration of an interleaved soft switching boost converter with an asymmetrical nine-level Cascaded H-bridge inverter for use in a photovoltaic system. The purpose of this system is to improve grid performance metrics related to power quality for photovoltaic sources while addressing power balancing issues. This converter structure is employed to optimize the efficiency of the photovoltaic power generating system and minimize switching losses with resonant soft-switching techniques. Applying an ANFIS-based control strategy enhances the dynamics of the DC-link voltage. For design and validation purposes, models in MATLAB/Simulink have been constructed for the proposed topology. The intelligent inverter developed obtains a peak efficiency of 93% at a unity power factor, with a total harmonic distortion of 3.56% in the output voltage. Unlike 5-level and 7-level Cascaded H-bridge multilevel inverter topologies, the comparison results empirically validate the proposed topology's stronger reliability. Moreover, with respect to the settling time, the proposed intelligent ANFIS controller demonstrated superior performance, achieving 0.3 seconds as compared to existing approaches like the PI controller

KEYWORDS: Asymmetrical Cascaded H-bridge Multilevel Inverter, Total Harmonic Distortion, Interleaved Soft Switching Boost Converter, Pulse Width Modulation, Photovoltaic Power Generation

1. INTRODUCTION

In today's environment, solar energy production has held an important position across several industries, and its role in power usage is extremely significant because it comes with a several demonstrated benefits, such as a robust framework, straightforward deployment, minimal upkeep, excessive energy storage, and a reasonable cost [1, 2].

In addition to these acceptable benefits, the technology has been the focus of numerous studies, who have conducted a lot of research on this Photovoltaic (PV) system and offered numerous unique concepts for the installation of grid-connected PV systems [3]. Despite these attractive benefits, the source voltage of PV is insufficient to satisfy the reference voltage, so the voltage that is produced by PV needs to be maximized in an effective manner [4, 5]. A DC-DC converter is designed to boost voltage gain, which eliminates the need for transformers and increases system dependability.

Increasing the voltage with the application of DC-to-DC converters is the critical procedure resulting in effectively using the PV source, and several converters have been utilised in the past to accomplish this [6, 7]. Boost converters had been employed in the beginning to increase voltage effectiveness, although the voltage obtained by these converters became unstable and failed to meet the grid voltage requirement. To maintain the system's overall voltage gain, a buck-boost converter, which is able to function in both buck and boost modes [8–10], is used. Although useful, this converter has several limits in terms of increasing the voltage-to-current ratio, which have been overcome by using Cuk SEPIC converters [11–15]. These converters have increased the number of values achieved; however, the produced voltage is insufficient for PV power generation.

A Dynamic Voltage Restorer (DVR) was employed to enhance voltage quality within the distribution system and utilizes three single-phase H-Bridge PWM inverters for each phase, strategically employed to lower the voltage rating of the series converters [16]. An

Interleaved Soft Switching Converter (ISSB) is used in this study to address all the aforementioned difficulties.

The energy production of this system is improved by recording the highest power obtained by employing typical MPPT approaches such as Perturb and Observe(P&O) and Incremental Conductance, which are not always effective [17–19]. As a result, a closed-loop control framework with a PI controller is developed to improve the efficiency and dependability of maximum power harvesting since it is able to extract the greatest amount of power [20]. The gain parameters for the PI controller have been obtained using the adoption of multiple algorithms, the most common of which is trial and error, but it provides inadequate performance, which has been resolved with the application of fuzzy logic control, which provides improved efficiency with severe time consumption [21]. As a result, the aforementioned concerns have been addressed with stabilised dynamic DC link voltage via the application of the ANFIS controller. The obtained DC voltage is not injected into the grid and needs to be converted into AC, which is efficiently accomplished through the use of an asymmetrical nine-level CHB MLI.

The converter generates the DC-link voltage, which is the inverter's input. Multilevel inverters have gained prominence in power applications in electronics due to their well-adapted ability to manage the rising demand for ratings of power and reliability resulting from fewer switches and reduced interference from electromagnetic waves. Increased frequency switching PWM in multilevel inverters has multiple benefits over a standard two-level inverter [22, 23]. As contrasted with 2-level inverters, MLIs produce superior sinusoidal output, cutting total harmonic distortion (THD) and thus decreasing filter demands while also having enhanced effectiveness, flexibility, and decreased strain across power electronic equipment.

The three traditional topologies of MLIs put forward in research are the Flying Capacitor (FC) [24] MLI, Neutral Point Clamped (NPC) [25] MLI, and Cascaded H-bridge (CHB) [26] MLI, each with various variants. The NPC architecture has the disadvantage of necessitating lots of clamping diodes with higher levels to create the output voltage waveform. FC MLI introduces the challenge of capacitor voltage equalisation and appears to be costly and problematic for a growing number of levels that require a large number of capacitors. An asymmetrical cascaded H-bridge inverter boasting 81 levels incorporates maximum power point tracking at the boost DC-DC converter stage, contributing to an overarching reduction in Total Harmonic Distortion [27].

Another inventive hybrid multilevel inverter design utilizes just 8 IGBT switches and 4 DC-link voltage sources can be adjusted using a 7-level model, incorporating 6 switches and 2 DC sources, connected in series with a half-bridge and the result is an output voltage with 21 levels, closely resembling a sinusoidal waveform[28].

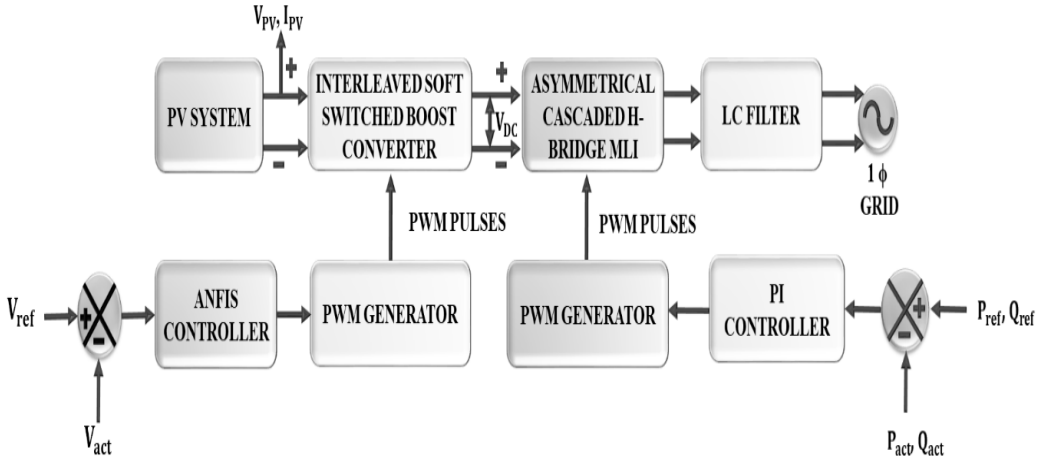
A control system based on fuzzy logic was introduced for accurate tracking, facilitating the integration of a photovoltaic (PV) system with an energy storage system through cascaded multilevel inverters [29].CHB MLI stands out in that it employs several DC sources, resulting in modularity that is able to be fed by a PV. When contrasted with other traditional topologies, CHB MLI requires fewer diodes and capacitors. This work proposes an asymmetrical nine-level CHB MLI for efficient DC to AC conversion.

In this research, an ISSB converter is used to acquire the necessary voltage, and the converter is controlled by the ANFIS algorithm. Efficient DC-to-AC conversion is achieved by employing an asymmetrical nine-level CHB MLI. The PI controller is used to achieve grid synchronization. The remaining sections of this study cover the following elements: the operation of the proposed system, the modelling of the PV module, the modelling of the ISSB converter, the ANFIS controller, and the modelling of the asymmetrical nine-level CHB MLI.

2. PROPOSED SYSTEM

The grid-connected PV system has gained popularity recently because of its durability, dependability, and ease of use. Furthermore, the ability of a grid-connected inverter to function even under unusual grid conditions, such as variations in voltage and frequency, relies heavily on the control strategy's robustness. For this reason, the work done on a 9-level Cascaded H-Bridge multilevel inverter (CHB-MLI) for photovoltaic (PV) power generation employing an ANFIS controller shown in figure 1 is described in this paper.

Fig 1. Configuration of the PV system using ISSB converter and CHB MLI

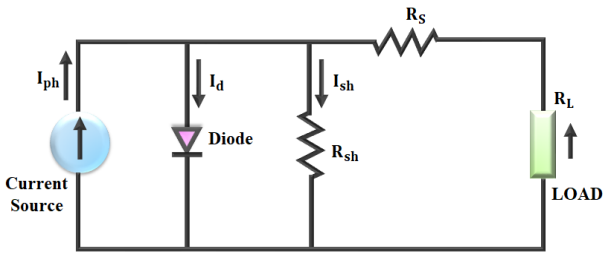


The interleaved soft-switched Boost converter is used in this proposed work to enhance the output voltage obtained from the PV system. The reference voltage is compared with the actual voltage that generates an error signal and is fed to the intelligent-based ANFIS controller. To regulate the proposed converter and to compensate for the error signal, the ANFIS controller is employed. The controlled output is delivered to the PWM generator, which has the ability to produce pulses for the better functioning of the converter. Furthermore, the DC-link voltage is given to the asymmetrical nine-level CHB MLI for converting the DC-AC supply. On the other hand, the actual power is compared with the reference power, which produces the error signal and is fed to the PI controller for error compensation. The required pulses for the superior operation of the inverter are attained by adopting the PWM generator. Finally, the uninterruptable and constant power supply without harmonics is delivered to the grid application with the aid of the proposed system.

3. PROPOSED SYSTEM MODELLING

3.1. Modelling of PV System

Fig.2. PV equivalent circuit



In a solar power system, several PV cells are connected in series and parallel to produce the necessary current or voltage. In essence, a large-area p-n junction semiconductor diode is a photovoltaic cell. Figure 2 depicts a simple PV cell equivalent circuit using the single diode technique. The output equation for a PV cell is expressed as

$$I_c = I_{ph} - I_0 = I_{ph} - I_{sat}\left[e^{\frac{q}{AKT_c}(V+IR_S)} - 1\right] \quad (1)$$

Where $K, T_c, R_S and\ A$ stand for the Boltzmann constant, temperature cell, stack internal resistance, and identity factor, respectively. The terms $I_{sat}, I_{ph}\ and\ q$ stand for photocurrent, electron charge, and PN junction reverse saturation current. A PV system is capable of producing the necessary amount of energy by taking into consideration the parallel and series panel combinations.

Using a suitable converter is capable of significantly improving the output from the PV panel; in this article, an ISSB converter is utilised.

3.2. Modelling of ISSB Converter

By interconnecting two or more switch converters in parallel, a technique known as interleaving; it is intended to improve the efficiency of the boost converter. As the number of stages increases, the ripple content decreases. In addition, soft switching techniques such as ZVS (zero voltage switching), ZCS (zero current switching), and resonant switching are utilised to minimise switching losses. Figure 3 depicts the proposed soft switching interleaved boost converter. Capacitors C_1 and C_2, output diodes D_1 and D_2, switches S_1 and S_2 and input inductors L_1 and L_2 make up the converter's primary structural components. Resonance components L_3 and C_3, parallel diodes D_3 and D_4, the diode of a resonance path D_5 and series inductors L_4 and L_5 make up the additional circuit. Additionally, the load resistor and the output capacitor are denoted by R_o and C_o correspondingly. Figures 3 and 4 show the conceptual waveforms and equivalents for each mode of operation, accordingly.

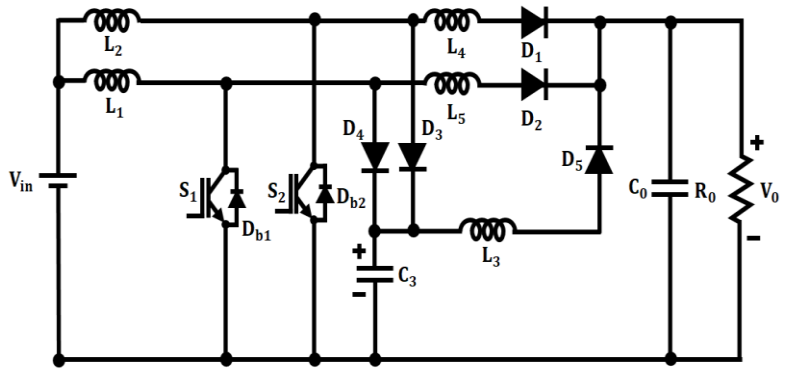


Fig.3. Proposed ISSB converter

Stage 1: $[t_0 - t_1]$

As seen in the figure 3(a), in mode 1, switch S_1 is switched on switch S_2 has been turned off and diodeD_{b2}, which is linked in parallel with the main switch S_2 is forward biased. The moment switch S_2 is activated this mode begins. S_2 is switched on during ZVS conditions since at t_0, voltage capacitor V_{C2} is zero and diode D_{b2} is forward biased. The current flowing via diode D_{b2} in this mode is equivalent to I_{L2}.

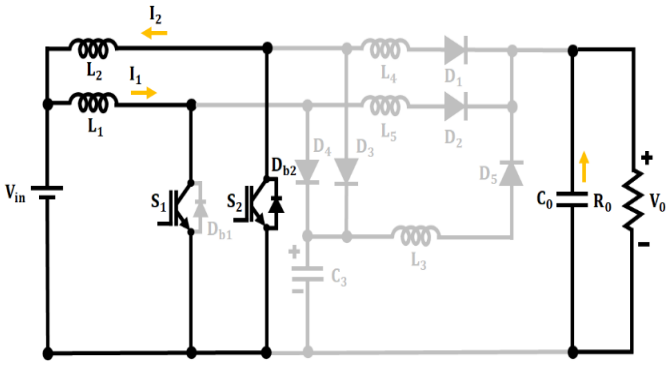


Fig. 3(a). Stage1

Stage 2: $[t_1 - t_2]$

After switch S_1 is switched off under ZVS conditions, the capacitor C_1 is linked in parallel with S_1 produces zero voltage at t_1, which triggers the beginning of this mode. When switch S_1 is switched off, a resonance occurs among inductor L_1 and capacitor C_3 via diode D_4. Additionally, a second resistance starts to exist across capacitor C_1 and inductorL_1. As a result, inductor L_1 transfers energy to capacitors $C_1$and C_3. As a result, capacitor voltages (V_{c1},V_{c3}) are expected to rise and inductor current (I_{L1}) decreases (seen in Figure 3(b).

i

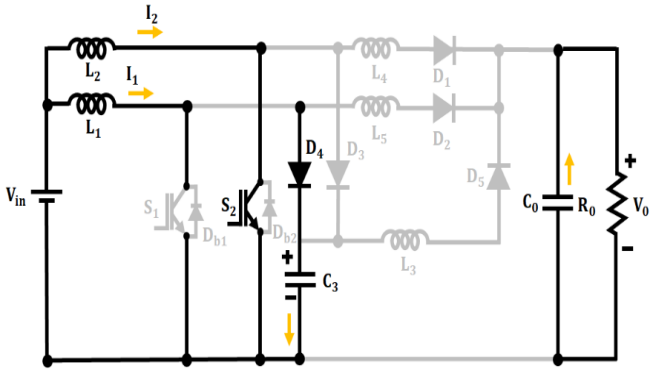
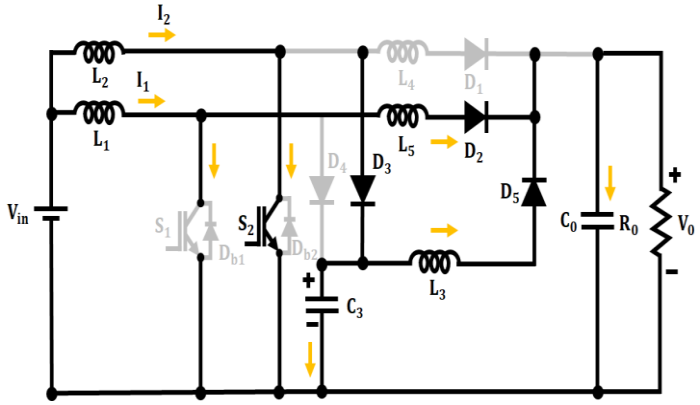


Fig. 3(b). Stage 2

Stage 3: $[t_2 - t_3]$

While diodes D_2 and D_5 are turned on at t_2 this state begins. There is currently no current flowing through inductors L_3 and L_5. These diodes are turned on under ZCS conditions at t_2 as a result of the series link between inductor L_5 and diode D_2 and inductor L_3 and diode D_5. Power is moved from the input to the output when diodes D_2 and D_5 are turned on (seen in Figure 3(c)).

Fig. 3(c). Stage 3



Stage 4: $[t_3 - t_4]$

Once the current through inductor I_{L1} becomes zero at t_3 and diode D4 is turned off, this mode begins. The novel resonance among capacitor C_1 and inductors L_1 and L_5 starts in this mode. As a result, inductor current I_{L1} rises while capacitor voltage V_{C1} falls (seen in Figure 3(d)).

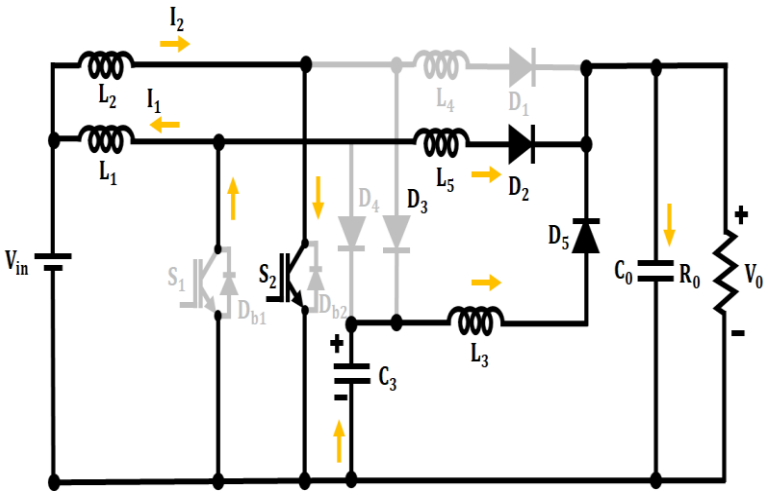


Fig. 3(d). Stage 4

Stage 5: $[t_4 - t_5]$

If diode D_2 is turned off at t_4 in the ZCS situation, this mode begins. This is carried out as a result of inductor current I_{L5} reaching zero at the start of this phase. Then, in ZCS circumstances, diode D_2 is turned off. The resonance among capacitor C_1 and inductor L_1 and capacitor C_3 and L_3 both persists in this mode. The resonant current that passes through C_3 and L_3 zeroes out at the end of this mode and diode D_5 is thus turned off in ZCS circumstances (seen in Figure 3(e)).

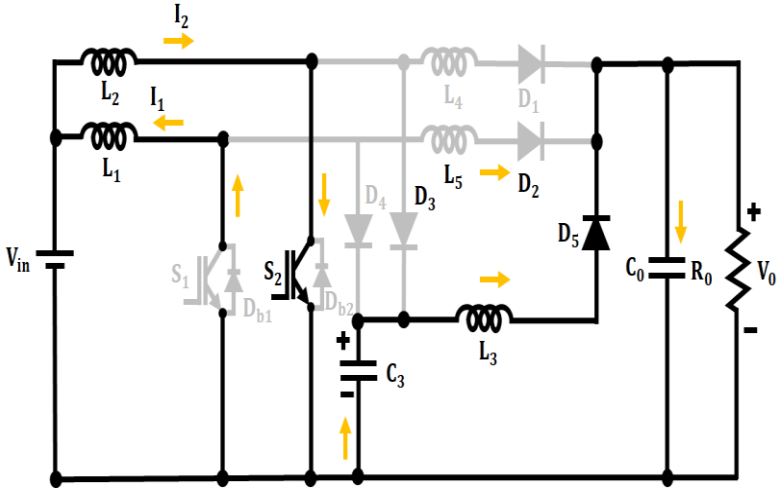


Fig. 3(e). Stage 5

Stage 6: $[t_5 - t_6]$

If diode D_5 is turned off under ZCS conditions, this state begins. Towards the end of this phase, when the capacitor voltage reaches zero, the resonance between C_1 and L_1 remains. Resonance between capacitor C_3 and inductor L_3 ends when diode D_5 is turned off. There is

no power flow from the input to the output in this mode. Also, the inductor current (I_{L2}) rises in a linear fashion. This mode ends when the ZVS criteria are met and the capacitor voltage V_{c1} drops to zero, turning on the diode D_{b1} (seen in Figure 3(f)).

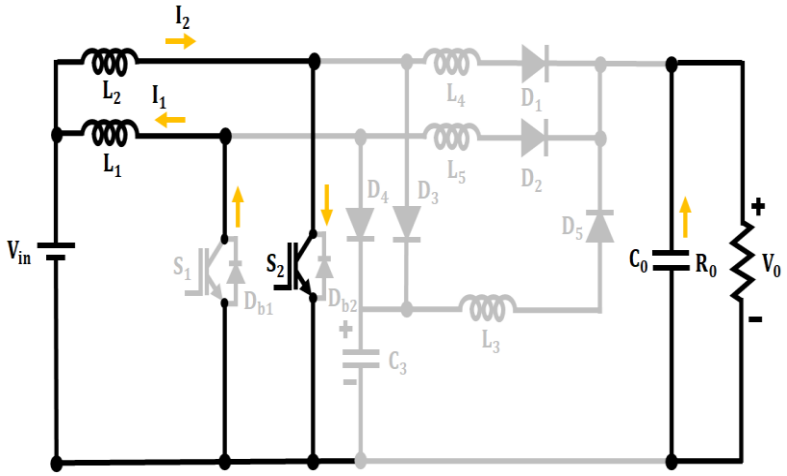
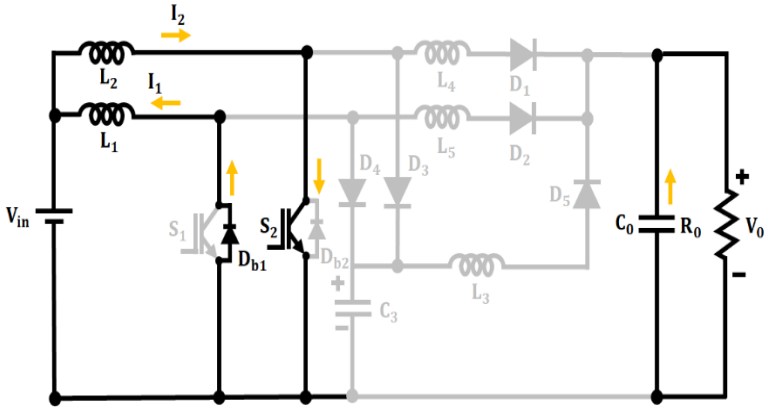


Fig. 3(f). Stage 6

Stage 7: $[t_6 - t_7]$

Whenever diode D_{b1} is turned on under ZVS conditions, this mode begins and clamps the voltage across capacitor C_1 to zero. Inductor current I_{L1} decreases linearly in this mode. Additionally, the output capacitor supplies the output power. Stated otherwise, there is no transmission of power from the input to the output. When diode D_{b1} is turned off under ZCS conditions and the inducer current I_{L1} drops to zero, this mode comes to an end. Additionally, at t_7, switch S_1 is activated under ZVS conditions (seen in Figure 3(g)).

Fig. 3(g).Stage7



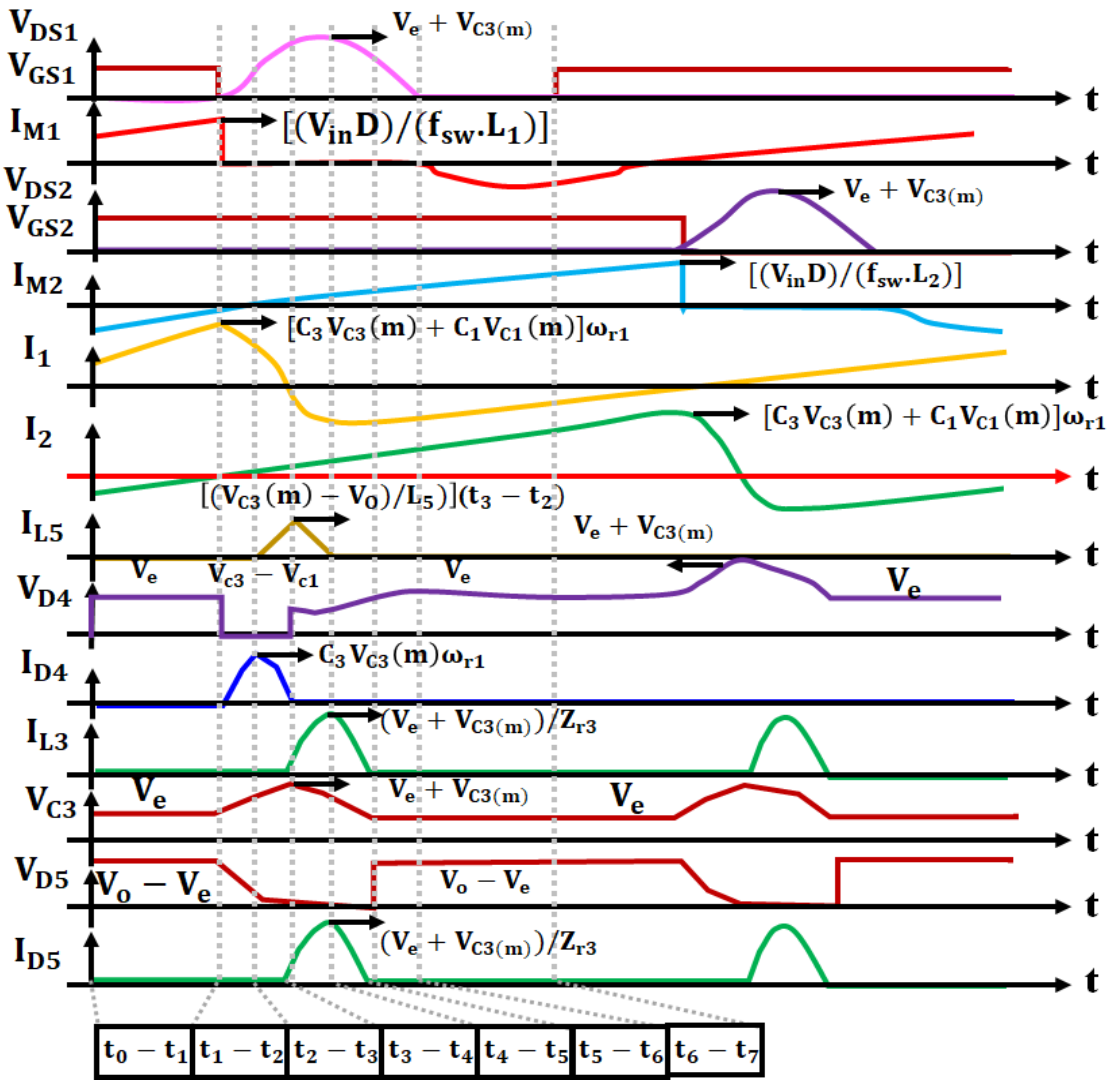


Fig. 4. Conceptual waveform of proposed ISSB converter

The forthcoming section provides a detailed description of the ANFIS controller for maintaining the constant DC link voltage.

C) MODELLING OF ANFIS CONTROLLER

Artificial intelligence control methods, such as FL and ANN, have been heavily utilised in a variety of industrial surroundings. These clever methods are not constrained by the mathematical presumptions of control theories and do not require a precise understanding of the system that has to be governed. By combining the benefits of ANN and FL methods, the control system's performance is intended to be enhanced. This study proposes the application of an ANFIS control method to monitor the DC-ink voltage of photovoltaic systems under various operating situations. Fuzzy reasoning and neural network learning are utilised by the ANFIS to manage uncertainty. In addition, there are other benefits associated with the ANFIS control strategy, including favourable and flexible tracking abilities with rapid convergence. The block diagram of the proposed ANFIS structure, which is based on a Takagi-Sugeno inference system, is displayed in Figure 5.

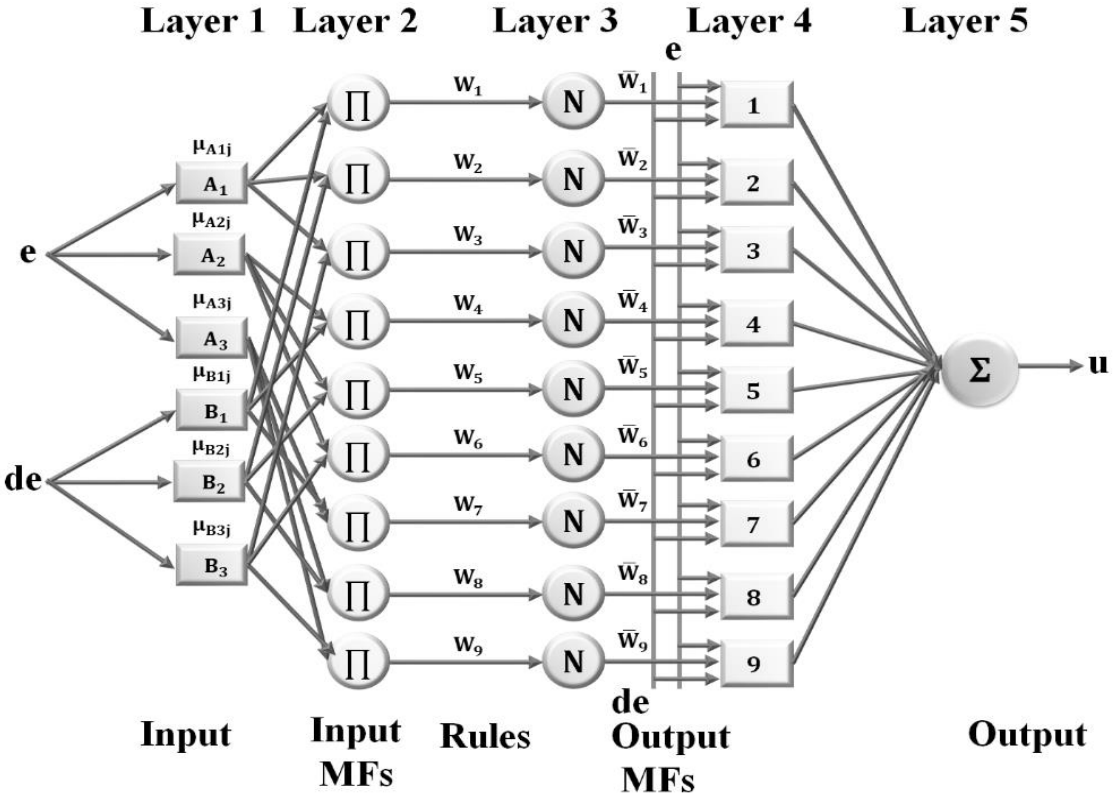


Fig. 5. ANFIS controller architecture

There are three membership functions (MFs) per input, two inputs, nine rules, one output, and five layers in the generated ANFIS. Specifically, the difference between the DC-link voltage reference and its observed value is one of the inputs ($e(k) = V_{dc-ref}(k) - V_{dc}(k)$), and the error change is the other input ($de(k) = e(k) - e(k-1)$). The output is the active power current component, which is divided by V_{dc} to obtain the active power reference p_{dc}. In fact, a detailed explanation of each layer is provided below.

Layer 1: The fuzzification layer is where the Membership functions are located. This layer applies membership functions to crisp input values such as (error x_1 = e) and (change in error x_2 = de) to derive fuzzy values. Fuzzy linguistic variables are described using generalized bell-shaped equations defined by parameters (a_i, b_i, c_i). These variables represent A_i and B_i. These functions can be called premise parameters as they define the degree of membership of the inputs to different fuzzy sets. The formula for the appropriate equation for each membership function is given as

$$\mu_{A_1}(x_1) = \mu_{B_1}(x_2) = \frac{1}{1+\left[\left(\frac{x_j - c_1}{a_1}\right)^2\right]^{b_1}} \quad (2)$$

$$\mu_{A_2}(x_1) = \mu_{B_2}(x_2) = \frac{1}{1+\left[\left(\frac{x_j - c_2}{a_2}\right)^2\right]^{b_2}} \quad (3)$$

$$\mu_{A_3}(x_1) = \mu_{B_3}(x_2) = \frac{1}{1+\left[\left(\frac{x_j - c_3}{a_3}\right)^2\right]^{b_3}} \quad (4)$$

If $x_1 = e, x_2 = de; x_j$, then x_j is equivalent to x_1 and x_2, where the variables sets are $(a_i, b_i$ and $c_i)$ and the linguistic labels are $(A_i$and $B_i)$. This layer's variables have been assigned as premise parameters.

Layer 2: Every node in this layer is represented by a circle with a label π. Every node in this layer calculates the firing strength of a fuzzy rule using the corresponding membership values from Layer 1 and multiplying them as per the logic. This multiplication supports the principle of "AND" fuzzy logic with two inputs on the given rule for a particular fuzzy logic set on a rule. This yields the unnormalized strength (ω_k) which indicates support towards the outcome of respective rules. It divides the input signals before sending them to layer 3 in accordance with the subsequent expression:

$$\omega_k = \mu_{A_{i,j}}(x_1).\mu_{B_{i,j}}(x_2) \quad (5)$$

Here, the subscripts k and j correspond to the numbers 1, 2... 9, respectively. Consequently, the firing strength is often referred to as the output of the each node.

Layer 3: This layer uses the total of firing strengths to enhance (normalize) individual rule firing power to achieve fair strength between rules.The output $\bar{\omega}_k$ ensures all strengths add up to one, thereby supporting that all fused strengths remain normalized to one. This method provides fair assessment power to the individual rules when the output from multiple rules is used together. In this layer, the normalized firing strengths of each rule are determined as follow:

$$\bar{\omega}_k = \frac{\omega_k}{\omega_1+\omega_2+..+\omega_g} \quad (6)$$

Layer 4: Each node calculates the output of its rule by using a linear function: $f_k = p_i x_1 + q_i x_2 + r_i$. The normalized firing strength from Layer 3 multiplies this function to scale it according to the importance of the rule. These parameters (p_i, q_i, r_i) are consequent parameters and are usually adjusted during the training process. Every node in this layer is a point of link to the node function, which is represented by the subsequent equation:

$$O_k^4 = \bar{\omega}_k f_k = \bar{\omega}_k(p_i x_1 + q_i x_2 + r_i) \quad (7)$$

p_i, q_i and $r_i$stand for the ensuing variables.

Layer 5: This layer adds up all the scaled rule results from Layer 4 to make the final system output. It does a weighted average of the single rule results based on their normalized strengths. The result is a clear value that shows the defuzzified output of the fuzzy inference system. It is determined by adding up all of the incoming signals in accordance with the phrase that follows.

$$u = \sum_{k=1}^{9} \bar{\omega}_k f_k \quad (8)$$

The consistent real power flow to the asymmetrical nine-level CHB MLI is ensured by adjusting the DC link voltage. As a result, the ANFIS controller is utilised in this study to modify the duty factor of the ISSB converter with the aim of keeping the dc link voltage stable.

D) MODELLING OF ASYMMETRICAL NINE-LEVEL CHB MLI

In this study, the CHB MLI is utilised for converting DC power into AC power and the output voltage produced by the asymmetrical nine-level CHB MLI is more than twice that of the DC source as seen Figure 6.This topology employs asymmetrical DC voltage sources and switches $S1, S2,$ and $S3$ produces various levels in the output waveform. The process has been referred to as the "level generating part" in this instance. By changing $S1', S2', S3'$ and $S4'$, the direction of the output waveform is inverted. This section is known as the "polarity production section." The circuit additionally includes three diodes ($D1, D2, and\ D3$) to establish current channels and to ensure that no short circuits happen. Figure 7 depicts the various operating modes of the proposed CHB MLI topology. Figure 7 (a, b, c and d) depicts the positive half cycle operating modes, whereas Figure 7 (e, f, g and h) depicts the negative

half cycle operating modes. The path of the current is shown by the bold line depending on the mode. For one full cycle, there are nine possible modes of current operation: four for every half cycle and one for zero. As a result, each mode is only entrusted with providing one output voltage level.

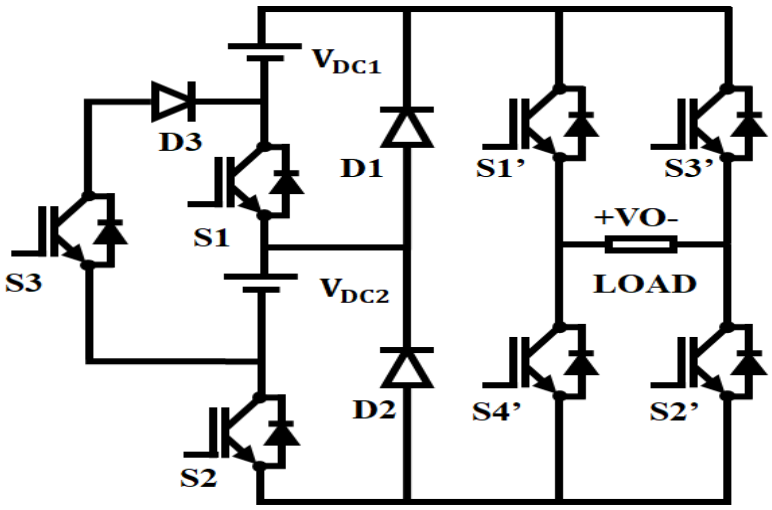


Fig. 6. Proposed asymmetrical Nine-level CHB MLI

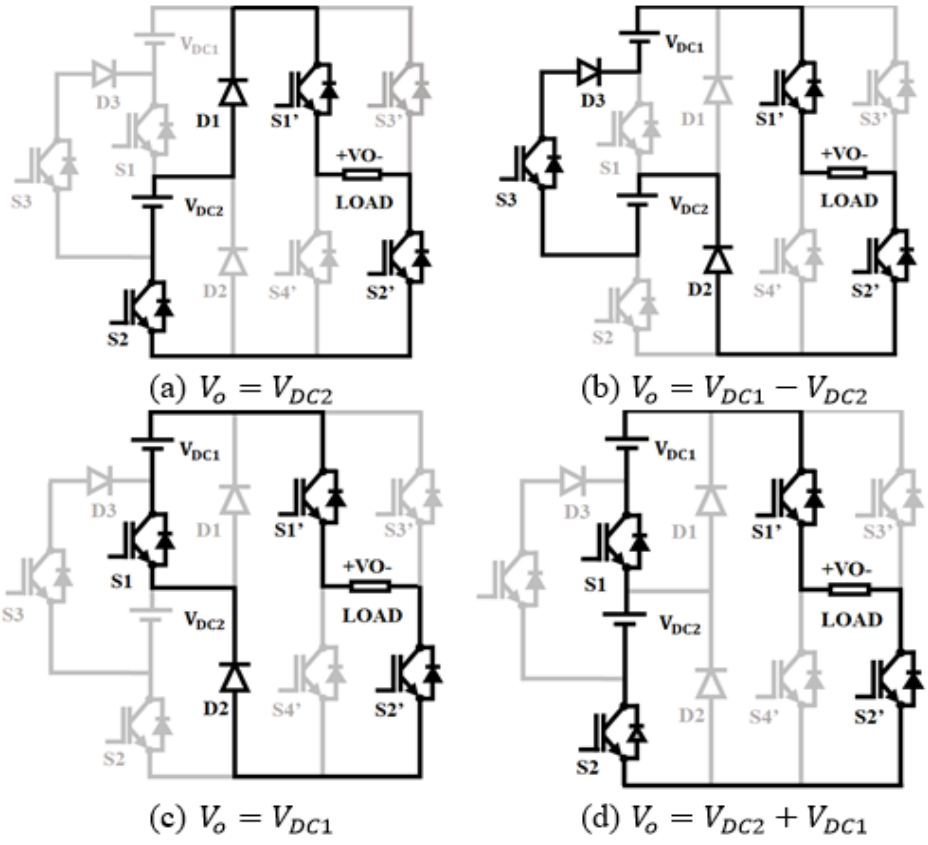


Fig. 7(a)-(d). Positive half cycle operating modes of proposed CHB MLI

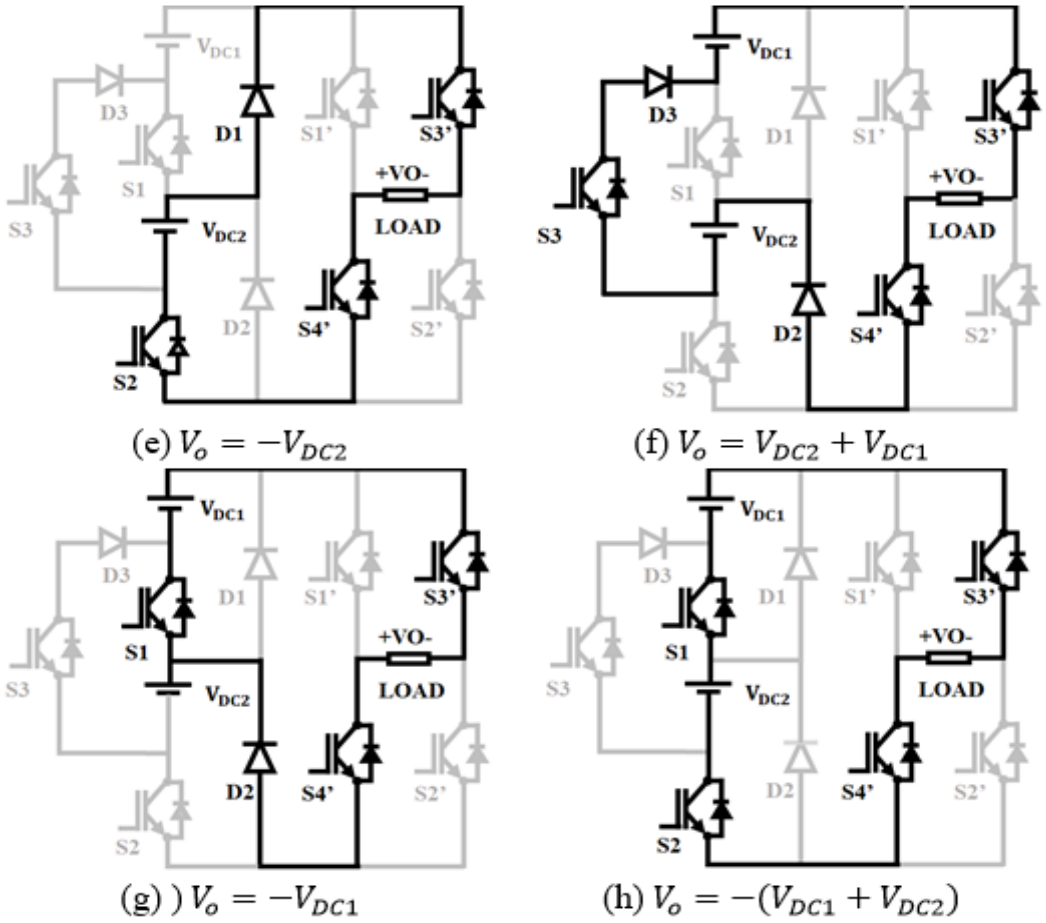


Fig. 7(e)-(h). Negative half cycle operating modes of proposed CHB MLI

Table 1. Switching states of proposed CHB MLI

		State Switches				
Mode	V_0	S_1	S_2	S_3	S_1', S_2'	S_3', S_4'
1	$V_0 = V_{DC2}$	0	1	0	1	0
2	$V_0 = V_{DC1} - V_{DC2}$	0	0	1	1	0
3	$V_0 = V_{DC1}$	1	0	0	1	0
4	$V_0 = V_{DC1} + V_{DC2}$	1	1	0	1	0
5	$V_0 = -V_{DC2}$	0	1	0	0	1
6	$V_0 = -(V_{DC1} - V_{DC2})$	0	0	1	0	1
7	$V_0 = -V_{DC1}$	1	0	0	0	1
8	$V_0 = -(V_{DC1} + V_{DC2})$	1	1	0	0	1
9	$V_0 = 0$	0	0	0	0	0

Table 1 shows the switch's conditions, whereby the numbers 1 and 0 denote whether the switch is ON or OFF. Modes I to 4 indicate the positive half cycle switching conditions, whereas modes 5 to 8 represent the negative half cycle switching conditions. The table also demonstrates that the operating pattern of the switches $S1, S2$, and $S3$ is identical in both half cycles. It also demonstrates that the switches $(S1', S2')$ function at opposing times to $(S3', S4')$.

The selection of ANFIS rather than simpler AI models is justified by its ability to learn in a hybrid way, that is, to combine the adaptive strengths of neural networks with the humanlike reasoning attributes of fuzzy logic. Nonlinearity and uncertainties in photovoltaic systems can be effectively handled by ANFIS as compared to traditional models. It offers faster convergence, more accurate regulation of the DC-link voltage, and better dynamic response. All these lead directly to improved power quality and reduced settling time which has been improved in the proposed system. Results so far achieved have been based purely on simulations in MATLAB/Simulink; hence actual performance under variable environmental and load conditions remains untested. This lack of experimental validation is quite a significant drawback and should be remedied in future work.

4. RESULTS AND DISCUSSIONS

In this research work, asymmetric nine level cascaded H- bridge multi-level inverter with an effective ANFIS controller for grid tied applications. By integrating interleaved soft switched boost converter, the output voltage is improved with reduced switching losses. Furthermore, a nine-level CHB MLI is effectively addressed the imbalance of power issue with greater power quality. The proposed topology is executed in MATLAB/Simulink and the comparative study is made over with the conventional approaches to foreshow the proficiency of the implemented system. The parameter specification is illustrated in table 2.

Table 2. Parameter ratings

Parameters	**Ratings**
Open circuit voltage	12V
Peak power	10KW, 10 panels
Number of cells connected in series N_s	36
Short circuit current	8.3A
Interleaved Soft switched Boost converter	
Switching Frequency	$10KHz$
L_1, L_2, L_3	$1mH$
C_1, C_2, C_2	$22\mu F$
C_o	$2000\mu F$
Diode	MCD95

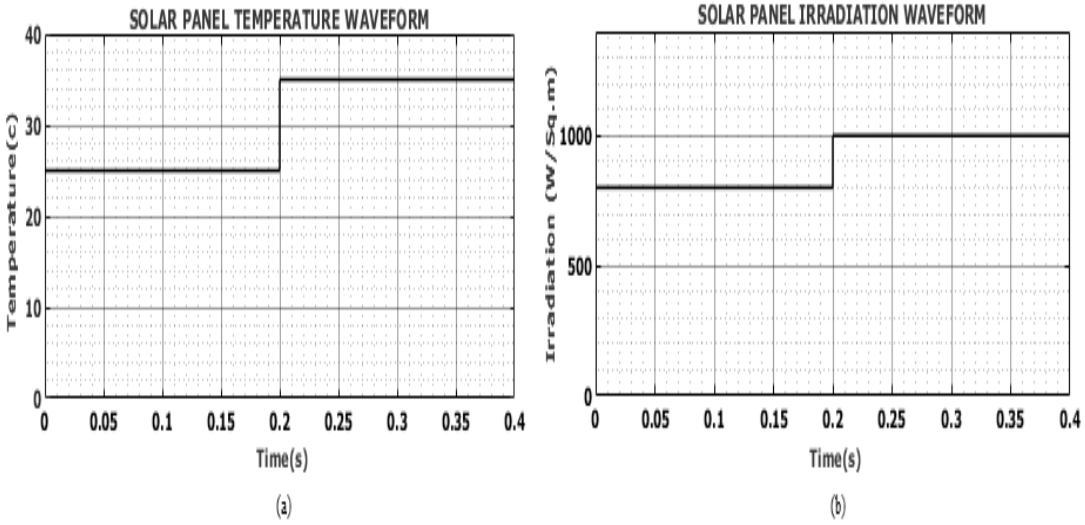
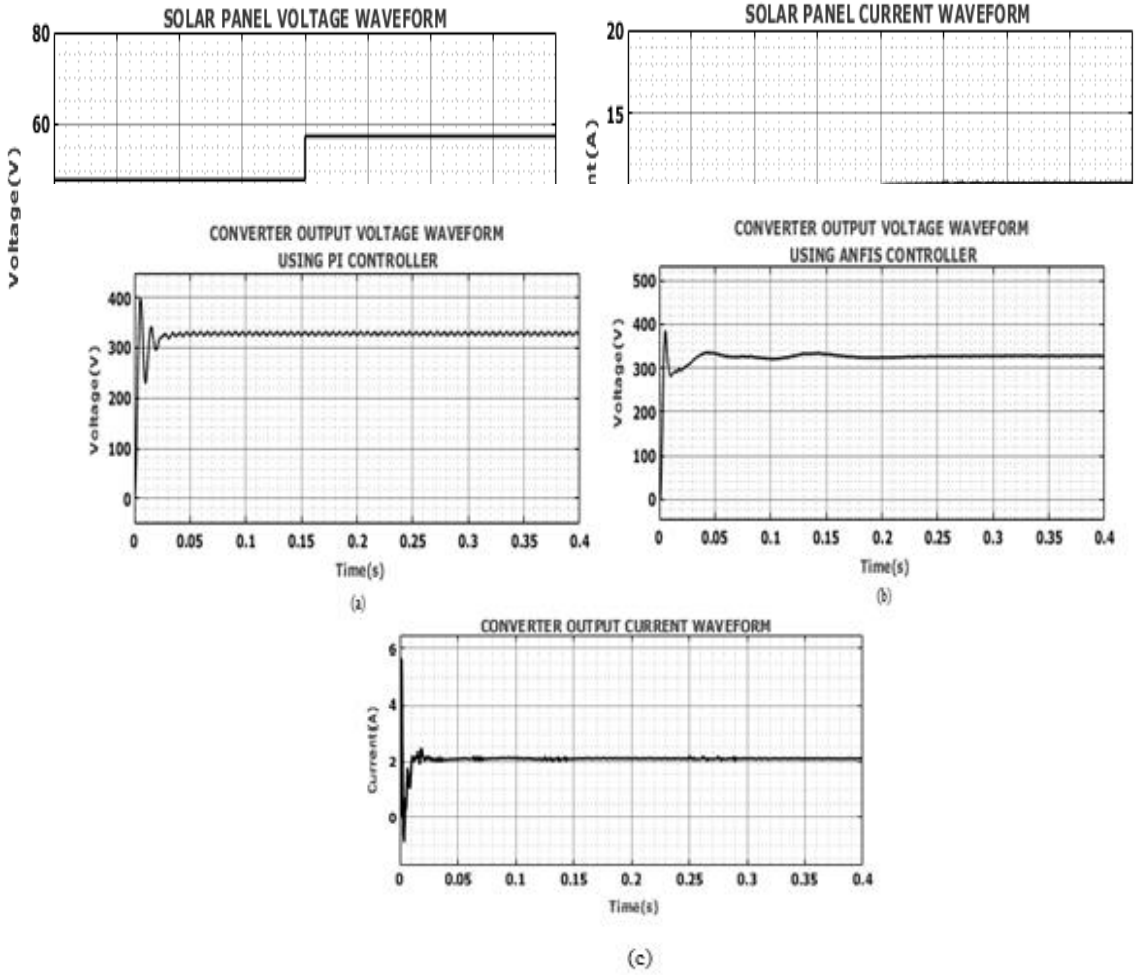


Fig. 8. Solar panel waveform (a) Temperature (b) Irradiation

Figure 8 represents the solar panel waveform for temperature and irradiation, which is analysed that initially the temperature gets fluctuated. After 0.2s it started to maintain constantly at $35°C$ respectively as illustrated in Figure 8(a). As illustrated in Figure 8(b), the irradiation gets fluctuated initially after 0.2s it constantly maintained at 1000(W/Sq.m).

Fig. 9. Solar panel waveform (a) Voltage and (b) Current

Solar panel voltage and current waveform is represented in Figure 9, from the Figure 9(a)



it is evident that the voltage gets oscillated initially with certain period of time, after 0.2s it continues to maintain constant voltage at 57V. Similarly, the current raised suddenly and fluctuated, which get constant current at 11A after 0.2s as specified in above Figure 9(b).

Fig. 10. Converter output voltage waveform using (a) PI and (b) ANFIS controller (c) Current waveform

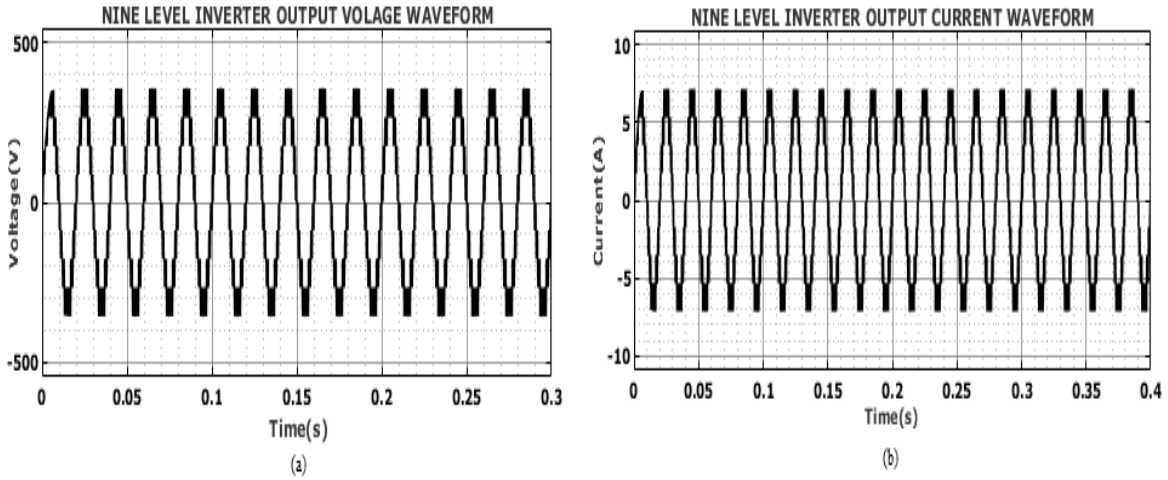
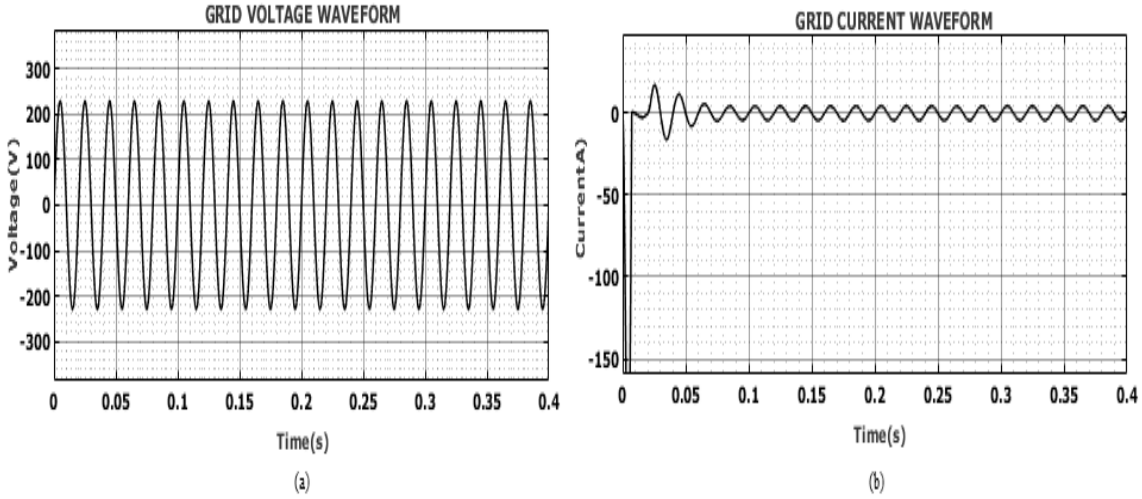


Figure 10 represents the converter output voltage waveform using PI and ANFIS controller, which is analysed that by using PI controller the voltage maintained with some distortions as shown in above Figure 10 (a). By using ANFIS controller, the voltage remains steady at 320V after 0.3s without any distortions as illustrated in Figure 10 (b). As represented in Figure 10(c), current gets fluctuated at certain period of time after 0.3s it constantly maintained at 2A without any distortions correspondingly.

Nine level inverter output voltage and current waveform is specified in Figure 11, from the Figure 11 (a) it is evident that the voltage gets constantly maintained at 350V to -350V. Similarly, the current is constantly maintained at 7A to -7A as represented in Figure 11(b).

Fig. 11. Inverter Output Voltage and current waveform

Fig. 12. Grid waveforms output (a) Voltage and (b) Current waveform



The grid voltage and current waveform is illustrated in Figure 12, from the result it is analysed that voltage is constantly maintained at 230V to -230V as represents in above figure 12(a). On the other hand, current is suddenly raised and maintained at 2A with distortions as illustrated in Figure 12 (b).

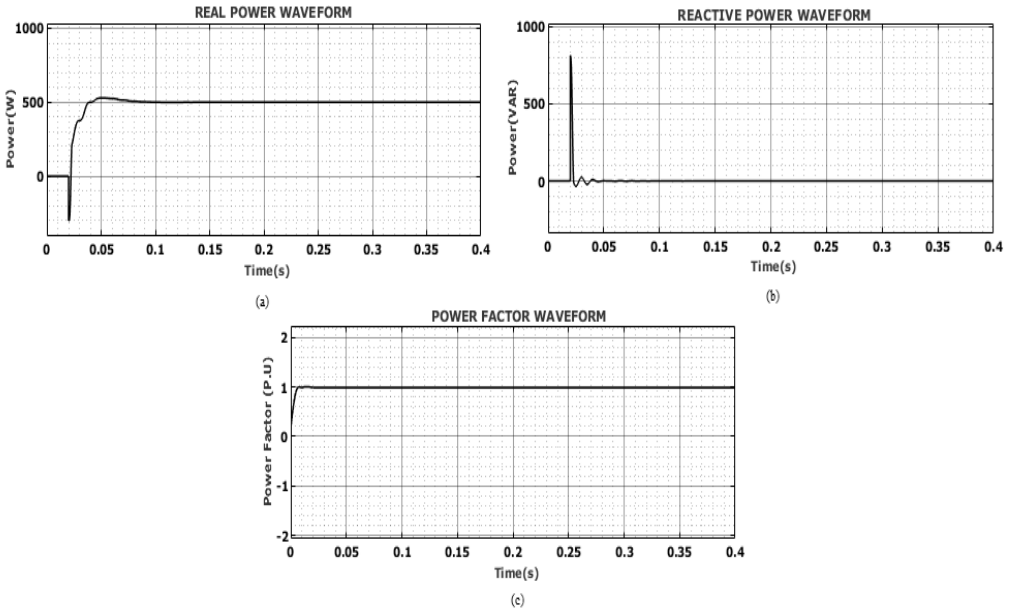


Fig. 13.Waveform for (a) Real power (b) Reactive power and (c) Power factor

Figure 13 represents the real power, reactive power and power factor waveform, which is observed that initially real power is suddenly raised with fluctuation and it is constantly maintained at 500(W) after 0.15s as specified in Figure 13 (a). Similarly, as illustrates in Figure 13 (b) the reactive power is raised suddenly and after 0.1s it is drop down with stable power at 0A. Moreover, the power factor is fluctuated initially after 0.01s it constantly maintained at 1(P.U) without any distortions respectively as seen in Figure 13 (c).

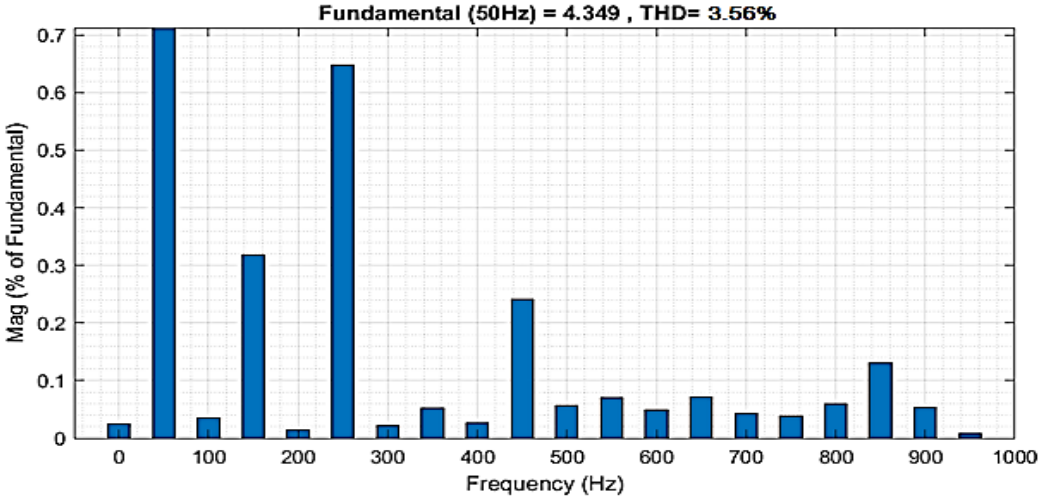


Fig. 14.THD waveform

The THD value waveform for the proposed asymmetrical Cascaded H-bridge MLI is represented in Figure 14, from the result it is observed that the proposed inverter attains 3.55% of THD value.

Table 3. Comparison of controllers

Controller	Rise time	Peak time	Settling time
PI	0.02	0.01	-
ANFIS	0.01	0.02	0.3

Table 3 provides a version of a comparison of the PI and ANFIS controllers based on dynamic performance values of rise time, peak time, and settling time. The values from Table 3 indicate that the ANFIS controller has lower rise and peak times as well as a settling time of just 0.3 seconds less than the PI controller. Overall, the data suggests ANFIS is quicker and more stable with respect to controller response. However, the PI controller settling time is absent, which complicates the comparison. The findings in this study have unevenness because the peak time can not be less than the rise time, and the PI settling time is absent. Numerical data validation will be obtained by extracting accurate numerical values from simulation plots in the future and validated with data markers. This will add a proper numerical foundation for the reliability of the controller comparison..

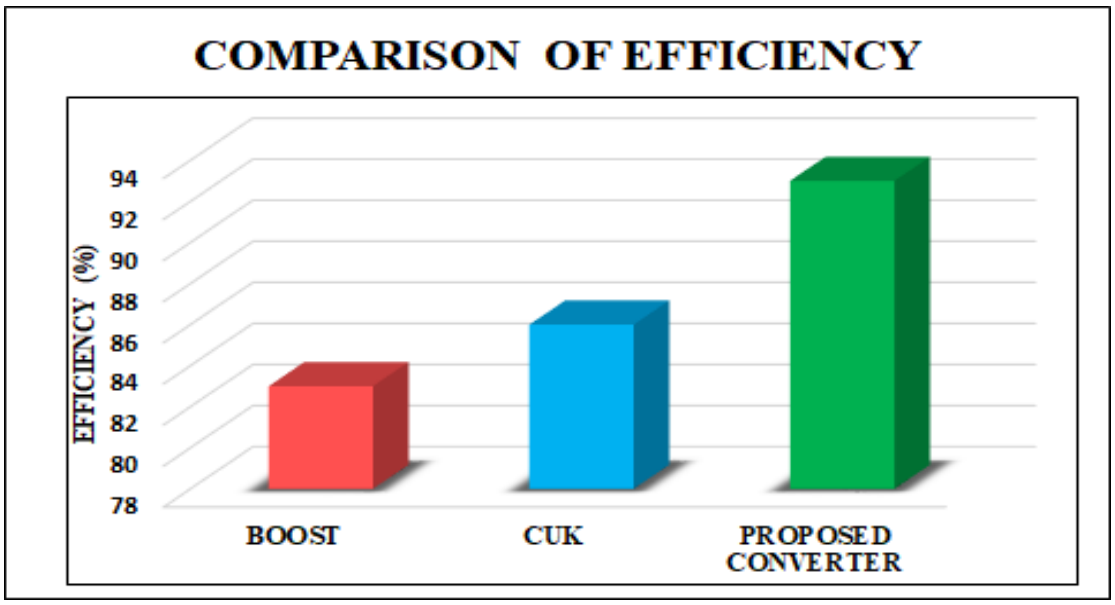


Fig.15. Comparison of efficiency

Comparison of efficiency is represented in Figure 15, which is evident that the proposed interleaved soft switched boost converter is compared with the conventional Boost and Cuk converter. From the graph it is analysed that the proposed converter has high efficiency of 93% compared to the existing converter approaches.

Inverters	THD (%)
5 LEVEL CHB MLI	16.66
7 LEVEL CHB MLI	9.47
PROPOSED ASYMMETRICAL 9 LEVEL CHB MLI	3.56

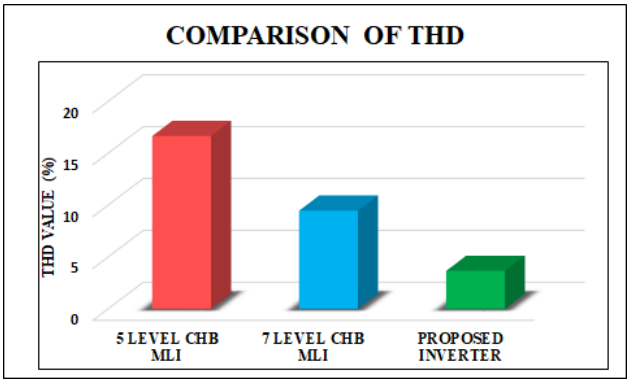


Fig. 16. Comparison of THD value

Figure 16 represents the comparison of THD value with the conventional and proposed inverter. The graph illustrates the proposed Asymmetrical 9 level CHB MLI achieves low THD of 3.56% compared to the other existing inverters like 5 level and 7 level CHB MLI topologies.

Table 4.Performance comparison of proposed method with other methods

Method	No. of levels	Switching losses	Efficiency	THD	Voltage stress on switches	Dynamic response
Conventional 5 level CHB inverter	5	High	88-90	7.5	High	Moderate
Conventional 7 level CHB inverter	7	Moderate	90-91	5.2	Medium	Moderate
Nine level CHB without interleaved boost	9	Moderate	91	4.5	Medium	Good
Proposed interleaved soft switching and 9 level CHB	9	Low	93	3.56	Reduced	Fast
NPC or Diode clamped inverter	5 or 9	Moderate	89-91	6.0	High	Slower than ANFIS

The proposed idea , using the interleaved soft-switching boost converter with a nine-level CHB inverter, has better efficiency (93%) and lower THD (3.56%) than traditional 5-level and 7-level inverters shown in table 4. The use of soft-switching which reduces both switching losses of the power devices and voltage stress. The interleaving further reduces the effective current ripple and the thermal dissipation. Using an ANFIS controller instead of the traditional approaches provides a much faster dynamic response and has a settling time of 0.3

seconds. The proposed topology is very promising compared to previous work in terms of efficiency, power quality and control response.

5. CONCLUSION

This research proposes an asymmetrical nine-level cascaded H-bridge multi-level inverter (CHB MLI) and an interleaved soft switching boost converter (ISSBC) for a photovoltaic (PV) power-generation system. The developed converter uses a resonant soft-switching technique to minimise switching losses and boost the efficiency of PV power-generating systems. By integrating a nine-level CHB MLI, superior power quality is attained without any power issues, which is a suitable DC/AC device for medium- and high-power applications, including renewable energy systems. Employing an ANFIS-based control technique enhances the dynamic performance of the DC-link voltage, and the proposed methodology is executed using MATLAB/Simulink. The comparative analysis is made over conventional topologies to demonstrate the proficiency of the developed work. As a consequence, the proposed converter attains a high efficiency of 93%, and by using the asymmetrical 9-level CHB MLI, the THD value is low (3.56%) compared with the other conventional approach. Moreover, the settling time of the proposed intelligent ANFIS controller has reached 0.3s more rapidly than the existing approaches. Results so far achieved have been based purely on simulations in MATLAB/Simulink; hence actual performance under variable environmental and load conditions remains untested. This lack of experimental validation is quite a significant drawback and should be remedied in future work.

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